Model 1793/6423
IEEE Standard 488 Output
Instruction Manual

KEITHLEY

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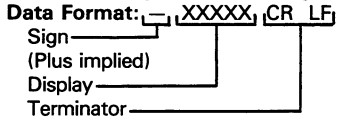
Instruction Manual
Model 1793/6423
IEEE Standard 488 Output

Cleveland, Ohio, U.S.A
Document Number 30535

SPECIFICATIONS

OUTPUT: 4½ digit ASCII data, sign, and overrange.

Data Format: 

Overrange Display: ASCII "OVER" in place of "XXXXX".

LOGIC LEVELS: Meets all IEEE Standard 488-1978 specifications.

MODES OF OPERATION: (Selected by internal switches).

Talk-Only: Allows user to connect meter to an IEEE-compatible listener. Data outputted at seven switch selectable rates from 2.5 rdgs/sec to 1 rdg/hr.

Addressable: Allows user to connect meter to an IEEE-compatible controller. Address selected by internal switches. Non-triggered addresses are even from 0 to 28. Triggered address is non-triggered address +1.

Non-Trigger: Upon receiving its trigger address, outputs the displayed reading.

Trigger: Upon receiving its trigger address, initiates a single A-D conversion and outputs the reading 400msec later.

ISOLATION: Digital outputs isolated from input circuitry ($10^{10}\Omega$, 40pF typ).

ENVIRONMENT:

Model 1793: Operate 0 to 55°C, 0 to 80% RH. Storage -25 to +70°C.

Model 6423: Operate 20°C to 30°C up to 70% RH. Storage -25°C to +55°C.

OUTPUT CONNECTOR: 24-pin IEEE-488 standard connector.

INSTALLATION: Field installable, mounts within and powered from meter. Adds 0.6kg (1.3 lbs). 10 watts.

Model 1793: Precludes 1788, 1792 installation.

Model 6423: Precludes 6428, 6422 installation.

ACCESSORIES AVAILABLE: 0.9m (3 ft.) IEEE Cable Keithley Model 7008-3, 1.8m (6 ft.) IEEE Cable Keithley Model 7008-6.

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SECTION 1
GENERAL INFORMATION

1.1 INTRODUCTION

The Keithley Model 1793/6423 IEEE-488 Isolated Output option provides all the logic and control functions necessary to interface the Keithley Models 177, 179, 179A, 179-20A, 480, and 642 to IEEE-488 bus. The Model 1793/6423 provides for triggered or non-triggered operation, with 4½ digit ASCII data, including sign and overrange indication, available over the bus. The Model 1793/6423 may be either field or factory installed.

1.2 FEATURES

Some important Model 1793/6423 features include:

1. Selectable Addressable or Talk–Only Modes. In the addressable mode, Model 1793/6423 data transmission may be controlled by an IEEE-488 compatible controller. In the talk-only mode, the interface may be used with an IEEE compatible listen-only device such as a printer.
2. Selectable Primary Address. The primary address is switch selected for any value between 0 and 29. An odd or even address selects non-triggered or triggered operation.
3. Adjustable Reading Rates. In the talk–only mode, the reading transmission rate over the bus may be set to a value between 2.5 readings per second and one reading per hour.
4. IEEE-488-1978 Standards. The Model 1793/6423 conforms to IEEE-488-1978 standards.
5. Secondary Addressing Capability. A secondary address, sent by a controller, controls trigger period as well as data string terminator sequence.

1.3 WARRANTY INFORMATION

Warranty information is located inside the front cover of this manual. Should it become necessary to use the warranty, contact your nearest Keithley representative or the factory to determine the correct course of action. Keithley Instruments, Inc. maintains service facilities in the United States, West Germany, Great Britain, France, the Netherlands, Switzerland, and Austria. Information concerning the application, operation, or servicing of your unit may be directed to the applications engineer at any of these locations. Check the inside front cover of this manual for addresses.

1.4 MANUAL ADDENDA

The information contained in this manual was believe to be accurate at the time of printing. Information concerning improvements or changes to the unit will be included on an addendum sheet included with this manual. Be sure to note any changes and incorporate them into the appropriate places in this manual before attempting to operate, install, or service the unit.

1.5 SAFETY SYMBOLS AND TERMS

The following safety symbols and terms are used in this manual or may be found on the instrument.

The  symbol on the instrument indicates that the user should refer to the operating instructions contained in this manual.

The symbol on the instrument indicates that a potential of 1000V or more may be present on the terminal(s). Use standard safety practices when such dangerous conditions are encountered.

The **WARNING** heading used in this manual explains dangers that could result in personal injury or death. Carefully read the associated information before performing the indicated procedure.

The **CAUTION** heading used in this manual explains hazards that could damage the instrument if the necessary precautions are not taken.

1.6 SPECIFICATIONS

Detailed Model 1793/6423 specifications are located at the front of this manual. Installation of the interface affects host instrument accuracy as described in Section 3, paragraph 3.10.

1.7 GENERAL OPERATING CHARACTERISTICS

The specifications listed at the front of this manual are performance standards or limits against which the Model 1793/6423 is tested. In addition to these specifications, several Model 1793/6423 operating characteristics are given below. These operating characteristics are not specifications, but they are typical characteristics or constraints which are included as additional information for the user.

1. Model 1793/6423 low output (pin 12 and 18 through 24 on J501) is to be connected to a ground point that is no more than 30V rms above earth ground.
2. Common mode input to the instrument must not exceed 10^5V•Hz to guarantee valid data output.
3. Model 1793/6423 IEEE-488 bus outputs are of open-collector configuration. These outputs have power-up/power-down protection to ensure that no invalid information is placed on the bus under these conditions.
4. The maximum data transfer rate for one reading is 1ms after the interface is addressed to talk.

1.8 INSTRUMENT AND INTERFACE COMPATIBILITY

1.8.1 Model 1793 Compatibility

The Model 1793 interface is compatible with the following instruments:

1. Model 177 DMMs with serial numbers 16500 and above.
2. Models 179 and 179-20A DMMs with serial numbers 24000 and above.
3. All Model 179A DMMs.
4. Model 480 Digital Picoammeters, serial numbers 12000 and above.

1.8.2 Model 6423 Compatibility

The Model 6423 is designed to be installed in Model 642 Electrometers with serial numbers 53402 and above.

1.9 UNPACKING AND INSPECTION

The Model 1793/6423 interface was carefully inspected, both mechanically and electrically, before shipment. Upon receiving the unit, carefully unpack it from the shipping carton and check for any obvious signs of physical damage. Report any such damage to the shipping agent at once. Retain the packing material in case future reshipment becomes necessary.

1.9.1 Model 1793 Shipments

The following items are included with every Model 1793 shipment:

- Interface Board Assembly
- Shield Assembly
- Replacement top cover for the host instrument.
- Model 1793/6423 Instruction Manual
- Additional accessories, as ordered.

1.9.2 Model 6423 Shipments

The following items are included with every Model 6423 shipment:

- Interface Board Assembly
- Shield Assembly
- Back panel assembly for the Model 642.
- Model 1793/6423 Instruction Manual.
- Additional accessories, as ordered.

1.10 PREPARATION FOR USE

1.10.1 Factory Installation

If the Model 1793/6423 was purchased with the instrument, it will be factory installed. No further preparation is necessary in this case before operation, which is covered in Section 3.

1.10.2 Field Installation

The Model 1793/6423 is easily installed in the field to upgrade instrument capabilities. See Section 5 of this manual for installation procedures.

1.10.3 IEEE-488 Primary Address

As shipped, the Model 1793/6423 is set for the addressable mode, with a primary address of 24 non-triggered operation, and a primary address of 25 for triggered operation. The mode or address may be changed as described in Section 3.

1.10.4 Line Voltage Selection

The Model 1793/6423 is designed to operate on either 115V or 230V power sources. The voltage is selected by a switch located on the interface board. See Section 5 for details.

1.11 SCOPE OF MODEL 1793/6423 INSTRUCTION MANUAL

This manual contains information for the operation, installation, and maintenance of the Model 1793/6423 IEEE 488 interface and is divided into the following sections:

1. Section 2 contains an overview of IEEE-488 bus operation.
2. Operating information, including addressable talk–only mode selection, primary address settings, and data format, is covered in Section 3.
3. A description of operating theory may be found in Section 4.
4. Section 5 contains servicing information, including installation procedures, verification of operation, and troubleshooting information.
5. A list of replaceable parts is contained in Section 6. Schematic diagrams and component layouts are located at the end of this section.

1.12 ACCESSORY CABLES

Accessory cables available to connect the Model 1793/6423 to the IEEE-488 bus include the Model 7008-3 and the Model 7008-6. The Model 7008-3 is 0.9m (3 ft) in length and has a standard IEEE-488 connector on each end. The Model 7008-6 is a similar cable 1.8m (6 ft) in length.

SECTION 2
AN OVERVIEW OF THE IEEE-488 BUS

2.1 INTRODUCTION

This section gives a brief description of the general bus structure. The information presented in this section is not intended to be a complete description of the IEEE-488 bus, which is also known as the GPIB (General Purpose Interface Bus). More complete information on the IEEE-488 bus may be obtained from the IEEE and a variety of other sources.

2.2 BUS DESCRIPTION

The IEEE-488 bus is an instrumentation data bus standardized by the Institute of Electronic and Electrical Engineers (IEEE) in 1975. In 1978, the standards were updated to their current revision and are designated as the IEEE-488-1978 standards. The Model 1793/6423 conforms to these standards.

The bus is a parallel data transfer medium designed to optimize data transfer without using an excessive number of lines. In keeping with this goal, the bus uses only eight data lines, which are used to transmit both data as well as some commands. Five bus management lines and three handshake lines round out the complement of bus signal lines.

2.3 BUS CONFIGURATION

Generally, there are two modes of operation for the bus. In the controlled mode, a central device such as a computer supervises bus operation by sending out commands to other devices. The bus may also be used without a controller in simpler applications. In this case, one device is dedicated as an output device, while one or more devices are configured as input devices.

A typical configuration for controlled operation is shown in Figure 2-1. The typical system will have one controller, as well as one or more instruments to which commands are given, and, in most cases, from which data is received. To properly identify each device by its capabilities, there are three catagories that describe device operation. These designations include: controller, talker, listener.

The controller does what its name implies: it controls other devices on the bus. A talker sends data, while a listener receives data. Depending on the instrument, a particular device may be a talker only, a listener only, or both a talker and listener (the controller will usually have talker and listener capabilities, depending on the application). The Model 1793/6423 has only talker capabilities; it is not able to either control or listen.

Any given system can have only one active controller (although control may be passed to an appropriate device through a special command), but any number of listeners and talkers may be connected up to the hardware constraints of the system. Generally, the bus is limited to 15 devices, including the controller, but that number may be reduced in some situations.

Before bus communications begin, the controller must command each device to listen or talk, as required. A number of devices may be commanded to listen simultaneously, but only one device may be an active talker at any given time. Otherwise, data transmission would be hopelessly garbled.

Before a device can talk or listen it must be sent a talk or listen command which is derived from its primary address. Normally, each device on the bus has a unique primary address so that each may be addressed individually. The primary address of the Model 1793/6423 is set to 24 at the factory (25 for triggered operation), but the address may be changed to other values between 0 and 28.

In addition to primary addressing, many devices make use of another addressing mode called secondary addressing. For example, the Model 1793/6423 uses secondary addressing to control triggering period and terminator sequence. When using this addressing mode with the Model 1793/6423, the secondary address must be received no later than 1ms after the primary address is transmitted.

Once the devices are properly addressed, appropriate bus transactions are set to take place. For example, once the Model 1793/6423 is addressed to talk, it will place its data string on the bus one byte at a time. The controller can then read this information and channel it to the desired location. With alternate programming, data may be transmitted directly from a talker to one or more listeners without going through the controller.

Once the data transmission sequence is complete, the controller sends special commands to clear the bus of any talkers or listeners. An UNT (untalk) command frees the bus of any talkers, and the UNL (unlisten) command cancels any listening action.

2.4 IEEE-488 BUS LINES

The signal lines on the IEEE-488 bus are grouped into three general catagories: data lines, bus management lines, and handshake lines. The data lines handle bus information, the bus management lines control the bus, and the handshake lines control the byte-to-byte transmission of information over the data lines. Each of these lines is active low with ap-

proximately 0V representing a logic 1. The following paragraphs describe the purpose of these lines, which are shown in Figure 2-1.

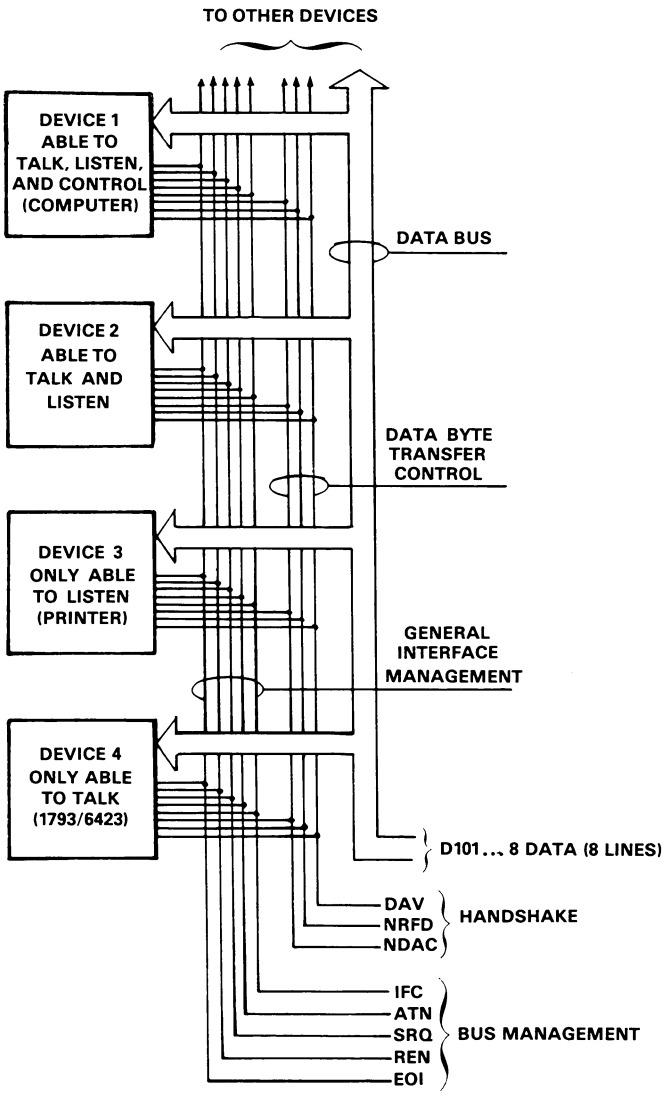

Figure 2-1. IEEE Bus Configuration

2.4.1 Data Lines

The IEEE-488 bus uses eight data lines that allow data to be received in bit-parallel, byte-serial fashion. These eight lines use the convention DI01 through DI08 instead of the more usual D0 through D7 terminology. DI01 is the LSB (least significant bit), and DI08 is the MSB (most significant bit). The data lines are bidirectional, but, of course, not all devices will require data transmission in both directions. Like the remaining bus lines, low is true.

2.4.2 Bus Management Lines

The bus management group is made up of five signals that act to ensure well-controlled bus operation. Bus management lines include:

1. ATN (Attention)—The ATN line is one of the more important bus management lines. The state of this line determines whether the data bus contains data or a primary or secondary address. When the ATN line is high, the data bus contains data, ATN is set low when a primary or secondary address is transmitted.
2. IFC (Interface Clear)—Setting the IFC line low causes the bus to go to a known state. The Model 1793/6423 responds to this condition by going into the talker idle state.
3. REN (Remote Enable)—Setting the REN line low sets up many instruments for remote operation. The Model 1793/6423 does not respond to REN.
4. EOI (End or Identify)—Setting the EOI line low is used to mark the end of a multi-byte data transfer sequence. The Model 1793/6423 does not implement EOI.
5. SRQ (Service Request)The SRQ line is set low by a device when it requires service from a controller. The Model 1793/6423 does not have SRQ capability.

2.4.3 Handshake Lines

The bus uses three handshake lines that operate in an interlocked sequence to ensure reliable data transmission regardless of the transfer rate. Generally, data transfer will occur at a rate determined by the slowest active device on the bus.

One of the three handshake lines is controlled by the source, while the remaining two lines are controlled by accepting devices. The three handshake lines are:

1. DAV (Data Valid)—The source controls the state of the DAV line.
2. NRFD (Not Ready for Data)—The acceptor controls the NRFD line.
3. NDAC (Not Data Accepted)—The acceptor also controls the NDAC line.

The complete handshake sequence for one data byte is shown in Figure 2-2. The sequence which follows is used for normal data as well as primary and secondary address transmission:

1. The source first places the byte to be transmitted on the data bus.
2. The source then checks to see that NRFD is high and NDAC is low from the previous transfer. If these conditions are not met, it is assumed that not all devices on the bus are ready, and the source must wait before proceeding. Because of the possibility of a bus hang up under these conditions, many controllers have time-out routines to display error messages if the transfer sequence stops for any reason.
3. Once the NRFD and NDAC lines are properly set, the source sets the DAV line low, indicating that the byte on the data bus is valid.
4. NRFD is then set low.

5. NDAC is then released by each device as it accepts the byte at its own rate. Once all devices have accepted the byte, NDAC goes high indicating to the source that all devices now have the current data byte.
6. The source now sets DAV high, indicating that the byte on the data bus is no longer valid.
7. NDAC then goes low.
8. NRFD is then released by each of the devices; when all devices have released NRFD, it goes high, and the bus is set to repeat the sequence with the next data byte.

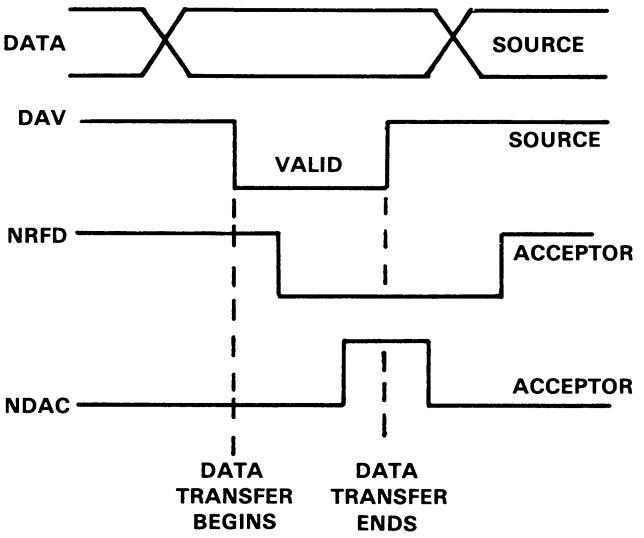

Figure 2-2. IEEE Handshake Sequence

SECTION 3
OPERATION

3.1 INTRODUCTION

This section contains information necessary to connect the Model 1793/6423 to the bus, select addressable or talk-only operation, and set the primary address. Also included is information on the data format and examples of controller programs.

3.2 BUS CONNECTIONS

The Model 1793/6423 is connected to the bus through a standard IEEE-488 connector and cable. The connector is designed to be stacked to allow a number of parallel connections on one instrument.

CAUTION
To avoid possible mechanical damage do not stack more than three connectors on one instrument.

Figure 3-1 shows a typical connecting scheme for the bus. Once the connections are made, the screws should be tightened securely. The Keithley Models 7008-3 and 7008-6 are ideal for this purpose. Alternately, custom cables may be constructed using the information in Figure 3-2 and Table 3-1.

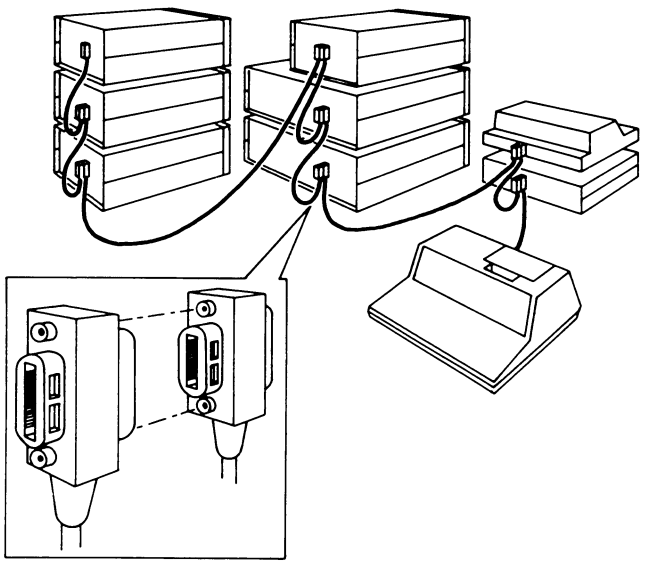

Figure 3-1. Typical IEEE-488 Connection Scheme

Table 3-1. IEEE Contact Designations

Contact Number	IEEE-488 Designation	Type
1	DIO1	Data
2	DIO2	Data
3	DIO3	Data
4	DIO4	Data
5	EOI*	Management
6	DAV	Handshake
7	NRFD	Handshake
8	NDAC	Handshake
9	IFC	Management
10	SRQ*	Management
11	ATN	Management
12	SHIELD	Ground
13	DIO5	Data
14	DIO6	Data
15	DIO7	Data
16	DIO8	Data
17	REN*	Management
18	Gnd	Ground
19	Gnd	Ground
20	Gnd	Ground
21	Gnd	Ground
22	Gnd	Ground
23	Gnd	Ground
24	Gnd, LOGIC	Ground

*Not used by Model 1793/6423.

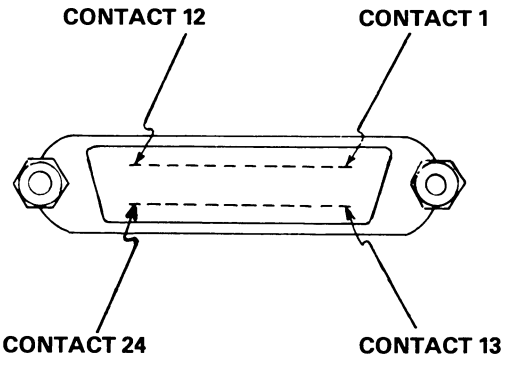

Figure 3-2. Contact Assignments

NOTE

The IEEE-488 bus is limited to a maximum of 15 devices, including the controller. The maximum cable length is 20 meters. Failure to observe these limits may result in erratic bus operation.

CAUTION

IEEE common on the Model 1793/6423 must not be connected to a voltage higher than 30V rms above earth ground.

3.3 MODE/ADDRESS DIP SWITCH

A DIP switch (S502) located on the interface board is used to select addressable or talk-only mode, the primary address in the addressable mode, and the reading rate in the talk-only mode. Switch configuration is shown in Figure 3-3. Figure 5-1 shows the location of the switch on the PC board.

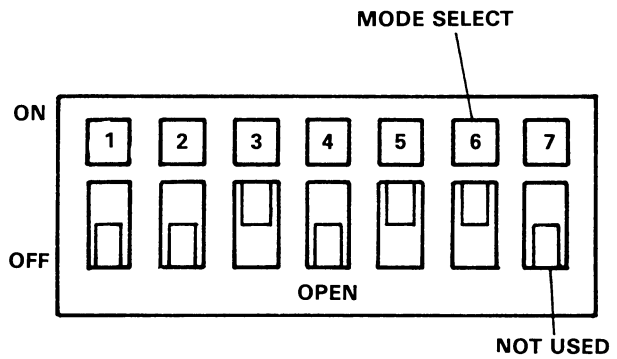

Figure 3-3. S502 Configuration

3.4 PRIMARY ADDRESS SELECTION

S6 on S502 selects the operating mode. S6 must be in the 0 (open) position for the instrument to operate in the addressable mode. When in the addressable mode, S2 through S6 determine the address of the interface, as summarized in Table 3-2. Note, that even addresses correspond to non-triggered opration, while corresponding odd addresses select triggered operation.

NOTE

As shipped, the Model 1793/6423 primary address is set to 24 for non-triggered operation and 25 for triggered operation.

3.5 ADDRESSABLE MODE OPERATION

When the instrument is in the addressable non-triggered mode (even primary addresses), it transmits the most recent reading over the bus immediately after receiving its primary address. The A/D converter is always in the run mode after the interface receives a non-trigger address. If a non-trigger address is received while the A/D converter is in the hold mode, a reading will not be transmitted until 400ms (1 conversion) later.

If the interface receives a trigger address (odd primary address), while the A/D converter is in the run mode, it will finish the present conversion and then complete one more. The reading from this last conversion is then transmitted over the bus, and the A/D converter is then placed in the hold mode. Each time a trigger address is received with the interface in the hold mode, a single A/D conversion will be performed, and the resulting data will be transmitted over the bus 400ms later. Table 3-3 shows the resulting time delays when going from one address mode to another. If a non-trigger address is received within 400ms of a previous non-trigger address, data will not be transmitted until the new conversion is completed.

Table 3-2. Primary Address Selection

Switch Settings (S502)							Non-Trigger Address (Always Even)	Trigger Address (Always Odd)
S7	S6	S5	S4	S3	S2	S1		
X	0	0	0	0	0	X	0	1
X	0	0	0	0	1	X	2	3
X	0	0	0	1	0	X	4	5
X	0	0	0	1	1	X	6	7
X	0	0	1	0	0	X	8	9
X	0	0	1	0	1	X	10	11
X	0	0	1	1	0	X	12	13
X	0	0	1	1	1	X	14	15
X	0	1	0	0	0	X	16	17
X	0	1	0	0	1	X	18	19
X	0	1	0	1	0	X	20	21
X	0	1	0	1	1	X	22	23
X	0	1	1	0	0	X	24*	25*
X	0	1	1	0	1	X	26	27
X	0	1	1	1	0	X	28	29

NOTE: X = Don't Care 1 = Closed 0 = Open
*Factory Setting

Table 3-3. Address To Address Time Delays

Condition	A/D Mode Before Output	A/D Mode After Output	Delay Until Bus Output
Power On	Run		
Non-Trigger Address Received	Run	Run	<1msec
Trigger Address Received	Run	Hold	400-800msecs
Trigger Address Received	Hold	Hold	400msec
Non-Trigger Address Received	Hold	Run	400msec
Non-Trigger Address Received	Run	Run	<1msec if >400msec since last address. 1 to 400msec if <400msec since last address.

3.6 SECONDARY ADDRESSING

An IEEE secondary address may be transmitted to the Model 1793/6423 to control the trigger period and terminator sequence. Because of the settling time of the A/D converter, it may be necessary to use secondary addressing to achieve triggered readings that are within rated accuracy of the instrument.

Secondary addressing may also be used to change the terminator from CR LF to LF CR for greater controller compatibility. Table 3-4 summarizes secondary addressing conditions. If no secondary address is sent, an address of 0 is assumed.

NOTE

The secondary address must be received within 1ms of the primary address, or it will be ignored.

Table 3-4. Secondary Address

Secondary Address	Triggered Period	Terminator
0	400msec	CR-LF
1	400msec	LF-CR
2	1.2sec	CR-LF
3	1.2sec	LF-CR

3.7 TALK-ONLY MODE

When S6 of S502 is in the closed position (logic 1), the Model 1793/6423 will operate in the talk-only mode. When in this mode, the interface will ignore talk commands sent over the bus, but will transmit its data string to an IEEE-488 compatible listen-only device such as a printer. While in the talk-only mode, the positions of S1, S2 and S3 determine the data output rate, as summarized in Table 3-5. S4 and S5 do not affect operation during this mode.

3.8 DATA FORMAT

Data transmitted over the bus is in the form of ASCII characters. The general format of the data string is shown in Figure 3-4. Numeric data is transmitted without decimal point, Also, note that, the display reading is replaced with "OVER" during an overrange condition.

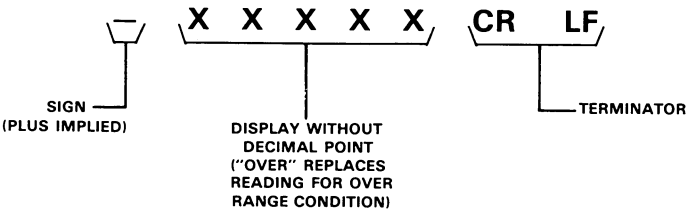

Figure 3-4. Data Format

3.9 CONTROLLER PROGRAMS

The Model 1793/6423 is designed to be used with IEEE-488 compatible controllers over the bus. When the instrument is

Table 3-5. Switch Positions for Talk-Only Mode

S7	S6	S5	S4	S3	S2	S1	Output Rate	Output Interval
X	1	X	X	0	0	0	2.5 rdgs/sec	400msec
X	1	X	X	0	0	1	25 rdgs/minute	2.4sec
X	1	X	X	0	1	0	6 rdgs/minute	10sec
X	1	X	X	0	1	1	1 rdg/minute	1 Min
X	1	X	X	1	0	0	12 rdgs/hour	5 Min
X	1	X	X	1	0	1	4 rdgs/hour	15 Min
X	1	X	X	1	1	0	1 rdg/hour	60 Min
NOTE: X = Don't Care 1 = Closed 0 = Open								

addressed to talk, it will transmit its data string over the bus one byte at a time. The programs in the following paragraphs allow the user simple control of the Model 1793/6423 with the following controllers: the Hewlett-Packard HP-85 computer, the Apple II computer, and the PET-CBM 2001 series computer.

These programs are intended to be a simple aid to the user and may not suit specific needs. Each program assumes that the Model 1793/6423 primary address is at its factory default value of 24 (25 for triggered opertation).

3.9.1 Hewlett-Packard HP-85 Program

The program below obtains one reading from the Model 1793/6423 and displays it on the HP-85 CRT. The HP-85 must be equipped with the HP-IB interface and an I/O ROM. The program assumes the interface select code is at its factory default value of 7.

PROGRAM	REMARKS
10 CLEAR	Clear CRT.
20 ENTER 724;A$	Address Model 1793/6423 to talk; place data in A$.
30 DISP A$	Display data string on CRT.
40 END	End program.

Note: For triggered operation, change line 20 to read: ENTER 725;A$

3.9.2 Apple II Program

The program below will obtain one reading from the Model 1793/6423 and display it on the CRT. The Apple II computer must be equipped with an Apple II IEEE-488 interface. The program assumes that the interface is located in card slot #3 of the Apple II.

PROGRAM	REMARKS
10 D$=CHR$(4): Z$ = CHR$(26)	Define control characters.
20 HOME	
30 PRINT D$; "PR#3"	Set output to IEEE bus.
40 PRINT D$; "IN#3"	Define input from IEEE bus.
50 PRINT "RDX"; Z$;	Address Model 1793/6423 to talk.
60 INPUT A$	Input data string into A$.
70 PRINT D$; "PR#0"	Set output to CRT.
80 PRINT D$; "IN#0"	Define input as keyboard.
90 PRINT A$	Display data string on CRT.

Note: For triggered operation, change line 50 to read: PRINT "RDY";Z$;

3.9.3 PET/CBM Program

The program below obtains one reading from the Model 1793/6423 and displays it on the CRT. The PET/CBM 2001 series computer has a standard IEEE-488 interface and associated software, so no additional equipment is necessary for this application. One limitation of the PET/CBM, however, is that, once a device is addressed to talk, it must respond within 65ms, or the computer will proceed to the next BASIC instruction, missing the reading. Line 30 of the program shows a method that can be used to circumvent this problem.

PROGRAM	REMARKS
10 OPEN 1, 24	Assign primary address 24 to logical file #1.
20 INPUT #1, A$	Address Model 1793/6423 to talk; input data string into A$.
30 IF ST=2 THEN 20	If bus time out, go back and input again.
40 PRINT A$	Display data string on CRT.

Note: For triggered operation, change line 10 to: OPEN 1, 25.

3.10 EFFECT OF INTERFACE INSTALLATION ON ACCURACY OF HOST INSTRUMENT

When the Model 1793/6423 IEEE-488 output is used in conjunction with the Model 480, 642, 177, 179-20A, 179 and 179A, the following additional error must be added to the accuracy specifications because of increased internal temperature rise.

Model 177

Ranges	Additional Error
All DC Volts	0.01% + 1d
20Ω, 200Ω, 2kΩ	0.01% + 1d
20kΩ, 200kΩ, 2000kΩ	0.03% + 1d
20MΩ	0.04% + 2d

Models 179, 179-20A, 179A

Ranges	Additional Error
All DC Volts	0.02% + 1d
All HI Ohms	0.01% + 1d

Model 480

Ranges	Additional Error
1nA, 100nA, 10μA	0.2% + 5d
10nA, 1μA, 100μA, 1mA	0.2% + 0.5d

Model 642

Ranges	Additional Error
All DC Volts	0.03% + 5d
All DC Amps	0.03% + 5d
All Coulombmeter	0.03% + 5d

Warm-up: 2 hours to rated accuracy

SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

This section contains a brief description of Model 1793/6423 operating theory. Schematic diagram for the interface is located at the end of Section 6. Figure 4-1 is a flow chart of overall Model 1793/6423 operation.

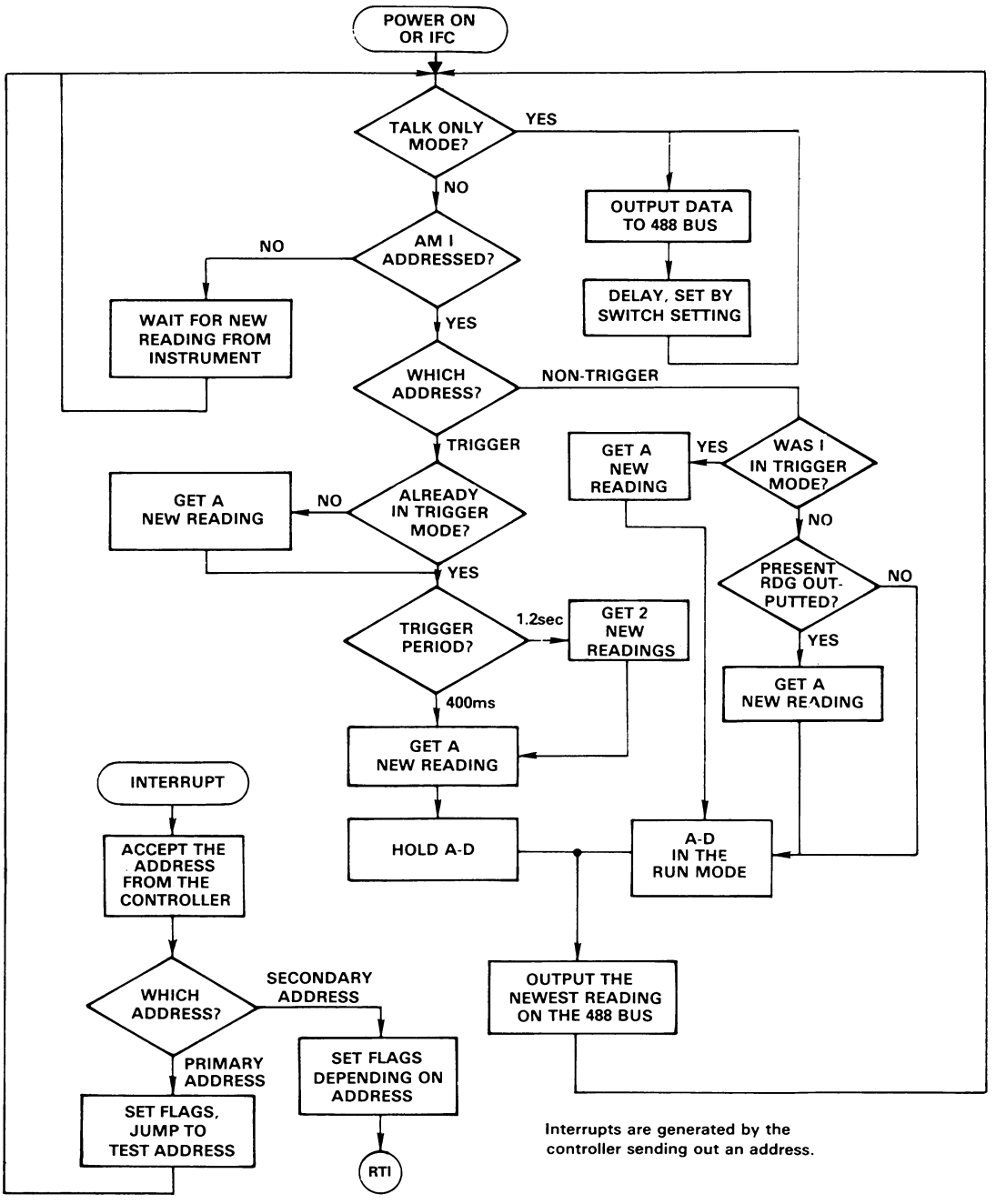

Figure 4-1. Model 1793/6423 Flow Diagram

4.2 OVERALL FUNCTIONAL DESCRIPTION

The Model 1793/6423 is controlled by a 6802 microprocessor (U511), 512 bytes of program memory (located in U512), and a PIA (U509). The microprocessor contains 128 bytes of RAM and an internal oscillator. The MPU internally divides this frequency by four to provide a 1MHz bus operating frequency.

The PIA (Peripheral Interface Adapter) provides the I/O necessary to convert isolated serial data from the instrument into parallel ASCII data. It also performs the handshaking necessary to control the IEEE-488 bus. Bidirectional data transmission is performed through port A.

The software that controls interface operation is stored in 512 bytes of ROM. The first 504 bytes are located at $8000 through $81F8, while the last eight bytes are the interrupt vectors located from $FFF8 through $FFFF.

4.3 POWER SUPPLY

The Model 1793/6423 has its own line-operated power supply. When the host instrument is turned on, K501 is energized, connecting the output of a bridge rectifier to a 5V regulator (VR501). The output of this regulator is used to power most of the ICs on the interface board. IC501, IC502 and IC503 are powered by the host instrument to maintain 1400V isolation between IEEE and instrument common.

4.4 MICROPROCESSOR RESET

When power is first applied, an RC network made up of C509 and R513 holds the MPU and PIA $\overline{\text{RESET}}$ lines low long enough to allow V_{cc} to stabilize. When the $\overline{\text{RESET}}$ line goes high, the PIA registers are cleared, and the MPU program counter is loaded with the reset vector to begin initialization.

4.5 PARALLEL TO SERIAL CONVERSION

Parallel BCD data from the instrument is converted, one digit at a time, into serial data which is sent through an opto-isolator and the PIA to the processor. The $\overline{\text{STROBE}}$ line, which is controlled by the A/D converter, pulses low once for each of the five BCD digits after an A/D conversion is complete (every 400ms). Timing for this process is shown in Figure 4-2.

U501, an eight-stage shift register, provides the actual parallel-serial conversion. This IC is controlled by the state of the P/$\overline{\text{S}}$ line. When P/$\overline{\text{S}}$ is high ($\overline{\text{STROBE}}$ low), the BCD digit, including overrange and sign bits, is latched into the register. When P/S goes low, serial data is clocked out Q8 at a 10kHz rate. Clocking for the serial shift-out process is provided by U503, which divides down the 100kHz clock from the host instrument.

The first bit shifted out Q8 is the P8 bit, which is permanently tied low. The second bit is P7, which is tied high. This bit acts as a sync bit to signal to the processor when to expect data. Bits P6, P5, P4 and P3 are the four bits of the BCD data, while P2 and P1 contain sign and overrange conditions respectively.

Three inverter sections of U502 provide sufficient drive capability for the LED contained in opto-isolator AT502. The opto-isolator output is used in the emitter follower configuration to provide a uniform turn-on turn-off time of approximately 20μs. Because data is transmitted asynchronously, the absolute times are not critical.

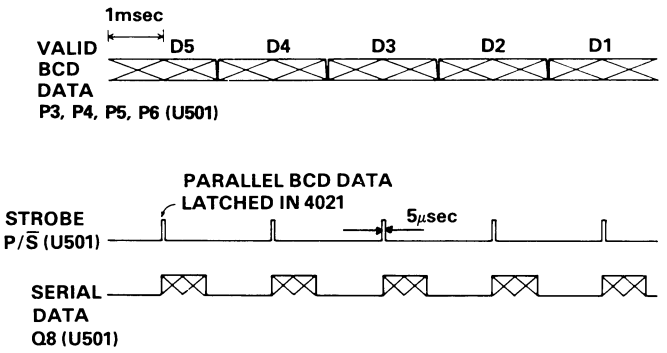

Figure 4-2. Timing Diagram

4.6 SERIAL TO PARALLEL CONVERSION

On the processor end, the incoming serial data must be converted into ASCII digits representing the transmitted reading. Data coming from the opto-isolator is applied to PB7 of the PIA. The processor continually monitors this line until it goes high, indicating the sync bit was received. After receiving the sync bit, the MPU monitors PB7 at 100μs intervals to sense the serial data bits as they come down the line. Once the overrange bit (P1) is received, the processor again waits for another sync bit. This process is repeated for a period of 10ms until all five digits of the latest reading are read and stored in memory.

4.7 A/D CONVERTER CONTROL

When the interface is addressed with an appropriate odd address, it will place the instrument into the trigger mode. This is achieved by setting the RUN/$\overline{\text{HOLD}}$ control line low. On the PIA side, CB2 provides the control signal, which is routed through inverter U507E before being applied to the opto-isolator, AT501. On the opposite side of the isolator, the signal is again inverted by U502E before being applied to the RUN/$\overline{\text{HOLD}}$ line of the instrument.

4.8 ADDRESS DECODING

The 6802 is capable of addressing 64k bytes of memory. Since the Model 1793/6423 uses only a fraction of that amount, only partial decoding is required. Table 4-1 lists the addresses of the various devices in the interface. Since only partial decoding is used, each device will also respond to addresses other than those shown. For example, although the ROM is allocated the $8000-$81FF range, it will actually re-

spond to addresses in the $8000-$FFFF range. Thus, the interrupt vectors can be accessed at locations $FFF8-$FFFF.

Table 4-1. Device Addressing

Device	Address Range
RAM (Internal to MPU)	$0000-$007F
PIA (U509)	$0080-$0083
DIP Switch Buffer (U513)	$0100
ROM (U512)	$8000-$81FF

4.9 PRIMARY ADDRESS ACCEPTANCE

When in the addressable mode, the Model 1793/6423 must receive a talk command derived from its primary address before it will transmit its data string. The process of receiving the primary address is as follows:

1. The MPU monitors the state of the ATN line through PB6 of the PIA. When ATN is set low, U504 and U505 are configured to input data from the bus and monitor the state of the DAV line. NRFD and NDAC are set up as outputs. U506A is cleared to set NDAC low and NRFD high.
2. Once the DAV line is set low by the controller, the MPU reads the primary address byte from the data bus through U504 and the PIA.
3. PB1 is placed high to set U506A, placing NDAC high and NRFD low, indicating to the controller that the address byte has been accepted.
4. Once all the devices on the bus have accepted the byte, the controller will set DAV high to indicate that information on the data lines is no longer valid.

4.10 DATA TRANSMISSION SEQUENCE

If the primary address received agrees with the address set on the DIP switches, the interface will send the data string over the bus using the following sequence:

1. The MPU sets PB4 high. The action configures U504 to output data over the bus; it also configures DAV as an output and NRFD and NDAC as inputs.
2. DAV is set high by placing PB0 high. This indicates to the accepting device that information on the data lines is invalid.
3. The first byte in the data string is fed out the PA0-PA7 lines, through U504, to the DI01-DI08 lines of the bus.
4. NRFD is sensed, though PB3, until it goes high, indicating that all listeners are ready for data.
5. DAV is set low to indicate that data is now valid.
6. NDAC is sensed through PB2 until it goes high, indicating that all listeners have accepted the byte.
7. DAV is set high to indicate that data is no longer valid.
8. The above procedure is repeated for ech of the eight bytes in the data string, including the sign, five data characters, an the carriage return, line feed terminator sequence.

4.11 IFC RESPONSE

The IFC line is set low by the controller to clear the bus of any listeners or talkers. When IFC is low, the NMI line on the processor goes low, causing a non-maskable interrupt. The MPU program counter is then loaded with the NMI vector, and the interface is placed in the talker idle state.

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

This section contains installation procedures and troubleshooting information for the Model 1793/6423.

5.2 INSTALLATION PROCEDURES

The Model 1793/6423 may be easily installed in the field. The procedures for the two interface models are different because of differences in the host instruments. Procedures for both the Model 1793 and the 6423 are covered separately below.

5.2.1 Model 1793 Installation

The Model 1793 is designed to be installed in the following models: 177, 179, 179-20A, 179A and 480. The unit is line operated from its own power supply. Note that, the Model 1788 battery pack and the Model 1792 BCD interface cannot be used when the Model 1793 is installed. Refer to Figure 5-1 and install the Model 1793 using the following procedures:

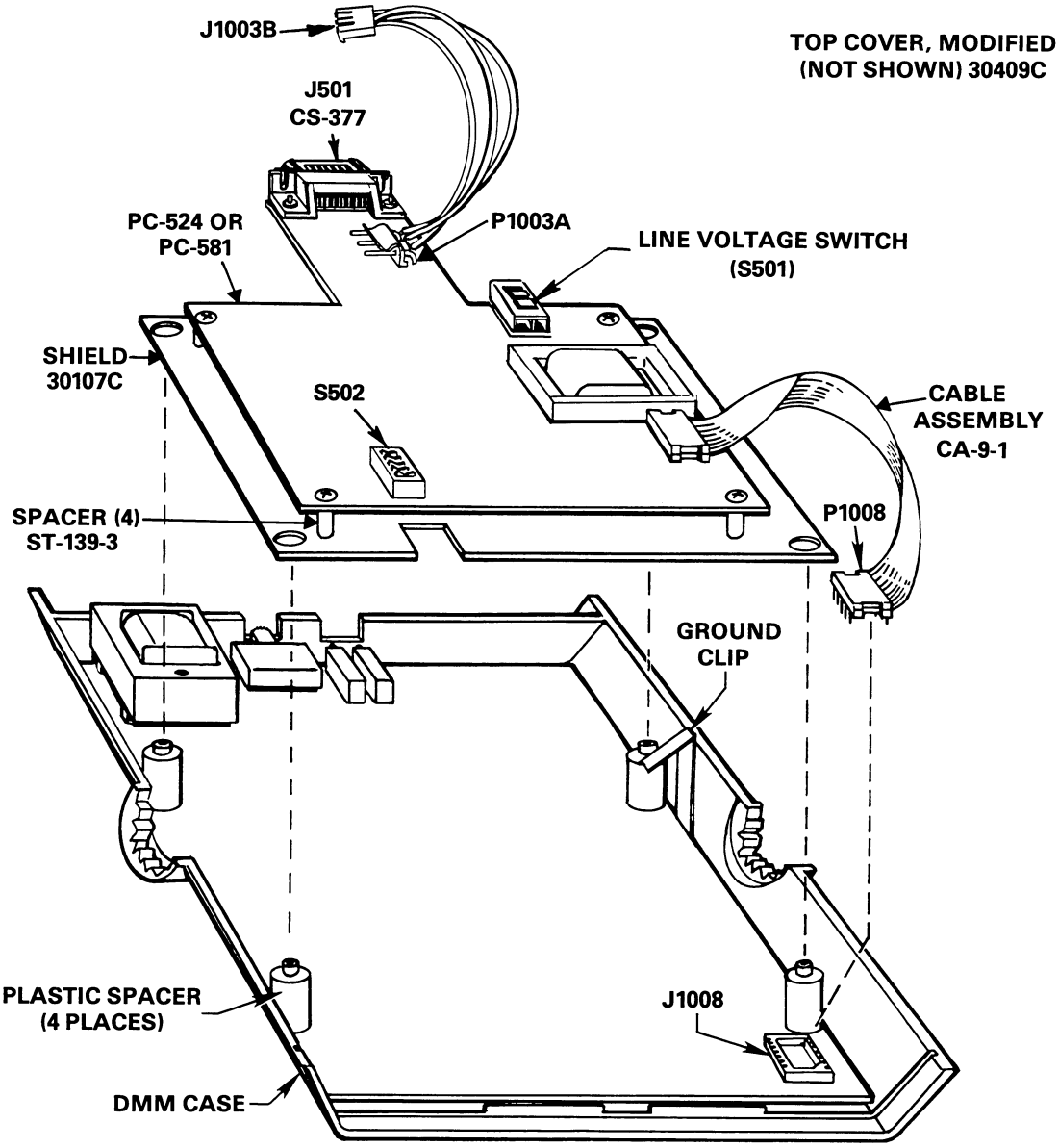

Figure 5-1. Installation Of Model 1793

WARNING

Disconnect the line cord and all test leads from the instrument before removing the top cover.

1. Turn the instrument bottom side up and remove the four screws in the bottom cover.
2. Hold the top and bottom covers together to prevent their separation and turn the instrument over to the normal position.
3. Lift off the top cover and set it aside. Remove the calibration shield and the Model 1788 Battery Pack or the Model 1792 BCD option, if installed. The four plastic spacers must remain in place on the main PC board.

NOTE

Do not discard the calibration shield, as this shield must be installed during instrument calibration, as described in the instruction manual for the instrument.

4. If the Model 1788 Battery Pack was removed, set the LINE/BAT switch on the main PC board to the LINE position.
5. Set the line voltage switch (S501) on the Model 1793 to the correct position (115 or 230V).

CAUTION

Operating the interface on the wrong line voltage may cause damage.

6. Disconnect J1003 from its mating plug on the instrument mother board (J1005 on the Model 480), and connect it to P1003A on the Model 1793. Connect J1003B to J1003 on the mother board (J1005 on the Model 480).
7. Connect P1008 to its mating plug on the mother board of the instrument (J1002 on the Model 480, J1008 on all others) as shown in Figure 5-1. Be sure to orient the ribbon cable as shown.
8. Install the Model 1793 in the instrument so that it rests on the plastic spacers. The shoulders must be projecting through the holes in the shield. Also, the ground clip must make contact with the upper side of the shield on the Model 1793.
9. As shipped, the Model 1793 is set for the addressable mode for use with a primary address of 24 (25 for triggerd operation). If the mode or address is to be changed, refer to Section 3 for the correct procedure. Functional verification may now be performed as described in paragraph 5.3
10. Install the new top cover that was shipped with the Model 1793. This cover has a hole at the back designed to accommodate the IEEE-488 connector. While installing the cover, be sure the front panel fits properly in the slots of both the top and bottom covers.
11. Once the top cover is properly seated, hold the two halves of the case together and turn the instrument over. Secure the covers with the four screws that were removed earlier.
12. Save all parts that were removed in case the Model 1793 is removed at a later date.

5.2.2 Model 6423 Installation

The Model 6423 is designed to be installed within the Model 642 Electrometer. The interface is powered by its own line-operated power supply. The Model 6422 BCD output or Model 6428 Battery Adapter cannot be used when the Model 6423 is installed. Refer to Figure 5-2 and install the Model 6423 as follows:

WARNING

Disconnect the line cord and all test leads from the instrument before removing the top cover.

1. Remove the four attaching screws and the top cover.
2. Remove and replace the back panel plate with the new plate that is furnished with the Model 6423. This plate has a slot to accommodate the IEEE-488 connector.
3. Remove the Model 6422 BCD option or Model 6428 Battery Adapter, if installed.
4. Remove the four attaching screws and replace them with the metal spacers, as shown in Figure 5-2. These spacers may fit snugly and require the use of a wrench to install them. Be careful not to cross thread or tighten them too tightly.
5. Connect P1008 to J1013 on the mother board. Be sure to orient the ribbon cable as shown in Figure 5-2. After making the connection, place the interface board outside the Model 642 so there is no strain on the cable. The board must be out of the way during installation of the shield and spacers in the next step.
6. Place the shield on the spacers with the nut plate on the bottom side; make sure the hole pattern is aligned as illustrated. Attach the shield to the spacers with the four screws as shown.
7. Install the four spacers on the shield.
8. Place the interface board on the spacers component side down and attach it with the four screws.
9. Attach the IEEE connector (J501) to the newly installed rear panel with the screws and #6 kep nuts supplied.
10. Disconnect the AC power connector at the mother board (J/P1006) and connect it to P1003A of the Model 6423. Connect J1003B to P1006 of the Model 642.
11. Set the line voltage switch (S501) to 115 or 230V, as required.

CAUTION

Operating the interface on an incorrect line voltage may cause damage.

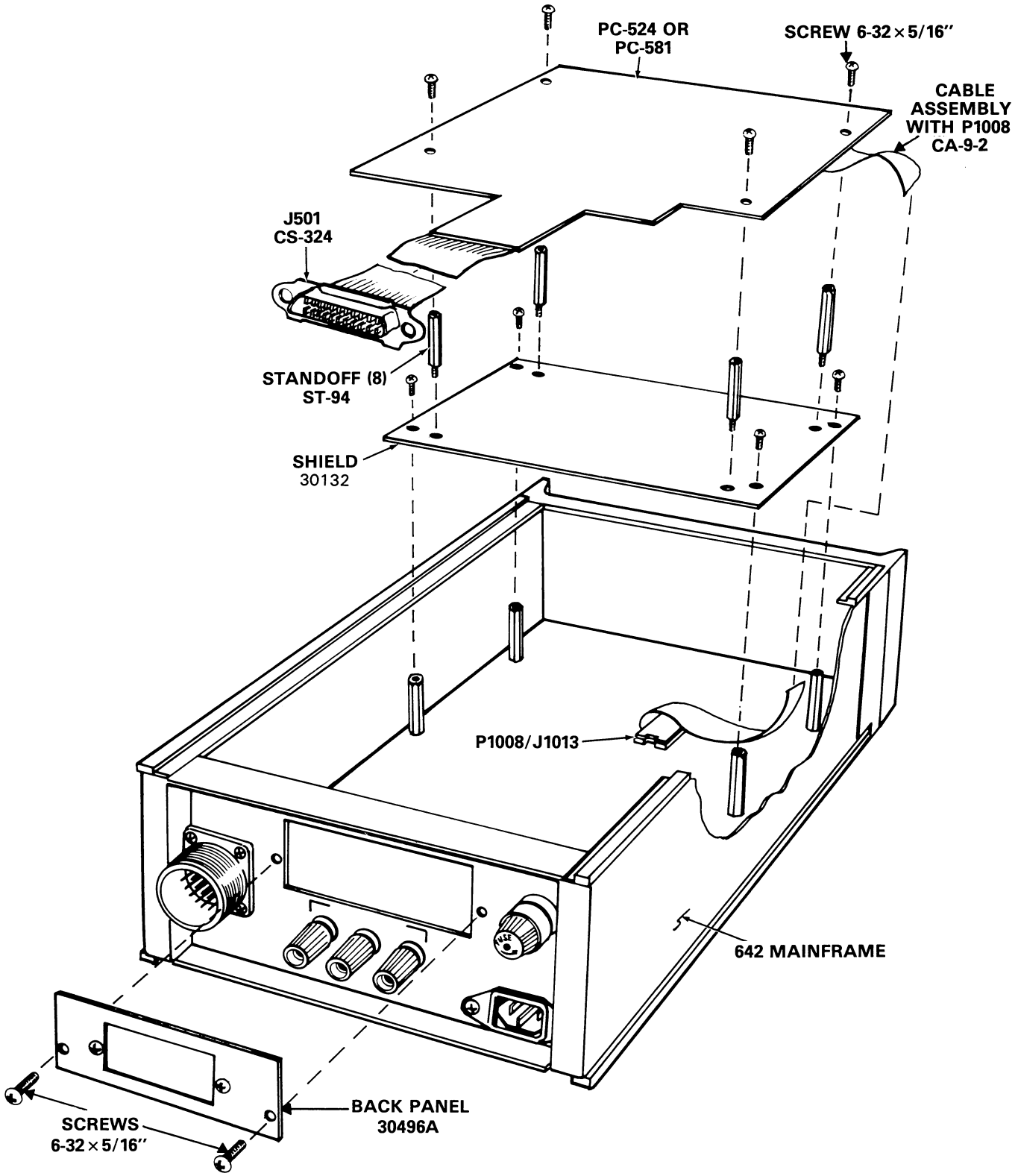

Figure 5-2. Installation Of Model 6423

12. Set the DIP switches (S502) for the proper mode of operation and timing/address as described in Section 3. Functional verification may now be performed as described in paragraph 5.3
13. Reinstall the top cover of the Model 642.
14. Save all removed parts in case the Model 6423 is removed in the future.

5.3 FUNCTIONAL VERIFICATION

Once the interface is installed, operation for both addressable and talk-only modes can be verified as described in the following paragraphs. If the top cover is installed on the instrument, it must be removed as described in the installation instructions in paragraph 5.2. After the verification procedure is complete, replace the top cover.

WARNING
Disconnect the line cord and test leads from the instrument before removing the top cover.

5.3.1 Addressable Mode Verification

To verify the Model 1793/6423 addressable mode, proceed as follows:

1. Set the instrument for the addressable mode and the desired primary address as described in Section 3.
2. Connect the Model 1793/6423 to a controller and apply power to the instrument.
3. Address the interface to talk with its even (non-trigger) primary address.
4. Confirm that the reading received and displayed by the controller is the same as that displayed on the instrument, less the decimal point.
5. Address the interface with its odd (trigger) address. Note that the data is delayed 400 to 800ms before being received by the controller. Once again, verify that the controller's reading agrees with the reading shown on the instrument, less the decimal point.

5.3.2 Talk-Only Mode Verification

1. Set the Model 1793/6423 to the talk-only mode and select the desired reading rate as described in Section 3.
2. Connect the interface to a listen-only device such as a printer.
3. Verify that the output rate agrees with the reading displayed on the instrument, less the decimal point.

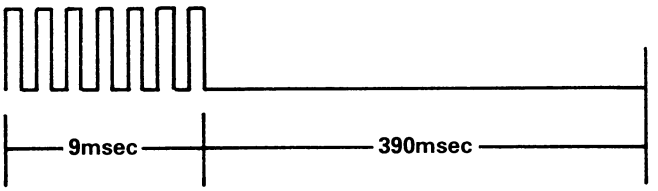

Figure 5-3. Isolated Serial Data

5.4 TROUBLESHOOTING INFORMATION

The Model 1793/6423 has four test points located on the interface board that can be used for troubleshooting. These points are described in Table 5-1. The top cover of the instrument must be removed, as described in the installation instructions, to allow access to these points.

WARNING
Disconnect the line cord and all test leads from the instrument before removing the top cover.

These points are marked on the interface board. Use the schematic diagrams and component layouts as an aid in locating these test points as well as for general troubleshooting information.

Table 5-1. Troubleshooting Data

Test Point	Signal	Reference
+5V	+5V Supply ±250mV	1793/6423 COM
TP1	STROBE-pulsed high 5 times (1 for each digit) every 400msec. The 5 pulses are 2msec apart. Refer to timing diagram for STROBE (Figure 4-2).	Instrument Input Low
TP2	ISOLATED SERIAL DATA-Approximately 9msec of positive going pulses occuring at 400msec intervals. The number of pulses is dependent on the displayed reading (see Figure 5-3).	1793/6423 COM
TP3	The system clock (Ø2) is a 1MHz, 0 to 4V square wave.	1793/6423 COM
Test Conditions: Instruments and 1793/6423 turned on. No controller attached.		

5.5 SPECIAL HANDLING OF STATIC-SENSITIVE DEVICES

CMOS and MOS devices are designed to operate at very high impedance levels. As a result, any static charge that builds up on your person or clothing can be sufficient to destroy these devices. Table 5-2 lists devices located on the Model 1793/6423 that might be destroyed by static charge. The precautions below should be observed when handling these devices to avoid possible damage.

Table 5-2. Static Sensitive Devices

Circuit Designation	Keithley Part Number
U501	IC-130
U502	IC-106
U503	IC-145
U507	IC-153
U509	LSI-8
U511	LSI-18

1. Handle and transport static-sensitive devices in static-protective containers. Typically, they will be received in containers of static-protective foam. Keep the devices in their original containers until ready for use.
2. Remove the devices from their protective containers only at a properly grounded work station, and only after grounding yourself with a wrist strap.
3. Handle the device only by the body; do not touch the pins.
4. Any printed circuit board into which the device is to be inserted must also be grounded to the work station.
5. Use only anti-static type solder suckers.
6. Use only grounded tip soldering irons.
7. Once the device is inserted into the board or socket it is adequately protected, and normal handling may resume.

CAUTION

The Model 1793/6423 is shipped in an anti-static bag. The interface board should be placed in this bag if it is to be removed from the instrument for any length of time.

SECTION 6
REPLACEABLE PARTS

6.1 INTRODUCTION

This section contains replacement parts information, schematic diagrams, and component layouts for the Model 1793/6423.

6.2 PARTS LIST

Electrical parts for the Model 1793/6423 are listed in Table 6-1. Mechanical parts are shown in Figures 5-1 and 5-2.

6.3 ORDERING INFORMATION

Keithley Instruments, Inc. maintains a complete inventory of all normal replacement parts. To place an order, or to obtain information concerning replacement parts, contact your Keithley representative or the factory. When ordering, include the following information:

- Equipment Model Number
- Equipment Serial Number
- Part Description
- Circuit Designation (if applicable)
- Keithley Part Number

6.4 FACTORY SERVICE

If the interface is to be returned to the factory for service, carefully pack it and include the following:

1. Complete the service form which follows this section and return it with the equipment.
2. Advise as to the warranty status of the equipment.
3. Write ATTENTION REPAIR DEPARTMENT on the shipping label.

NOTE

If the problem is known to exist in the interface rather than the host instrument, only the interface need be returned. However, if there is some question as to the location of the problem, both the interface and the host instrument should be returned for repair.

6.5 COMPONENT LAYOUTS

Physical locations of parts on the interface board are shown on one of the following component layout drawings, depending on the model number:

- Model 1793, drawing number 31465.
- Model 6423, drawing number 31479.

6.6 SCHEMATIC DIAGRAMS

Schematic diagrams located at the end of this section include:

- Model 1793/6423, drawing number 31469.

Table 6-1. Model 1793/6423, Parts List

Circuit Desig.	Description	Schematic Location	PC-Board Location 1793	6423	Keithley Part No.
AT501	IC, Optically-Coupled Isolator, FCD820	C-6	E-3	F-3	IC-82
AT502	IC, Optically-Coupled Isolator, FCD820	C-5	E-3	F-3	IC-82
C501	Capacitor, 4.7μF, 35V, Aluminum Electrolytic	A-4	D-2	E-2	C-179-4.7
C502	Capacitor, 4700μF, 16V, Aluminum Electrolytic	C-3	D-3	E-3	C-290-4700
C503	Capacitor, 0.1μF, 16V, Ceramic Disc	G-3	C-4	D-4	C-238-.1
C504	Capacitor, 0.1μF, 16V, Ceramic Disc	E-3	D-4	E-4	C-238-.1
C505	Capacitor, 0.1μF, 16V, Ceramic Disc	D-4	D-4	E-4	C-238-.1
C506	Capacitor, 0.1μF, 16V, Ceramic Disc	F-1	D-4	E-4	C-238-.1
C507	Capacitor, 22pF, 500V, Ceramic Disc	D-5	B-5	D-5	C-22-22p
C508	Capacitor, 22pF, 500V, Ceramic Disc	D-5	C-5	D-5	C-22-22p
C509	Capacitor, 4.7μF, 35V, Aluminum Electrolytic	E-5	D-5	E-5	C-179-4.7
C510	Capacitor, 0.02μF, 500V, Ceramic Disc	B-3	B-3	C-3	C-22-.02
CR501	Bridge Rectifier, Silicon, 1.5A, 400PIV	B-3	D-3	E-3	RF-46
CR502	Diode, Silicon, 1N4148	B-4	C-3	D-3	RF-28
CR503	Diode, Silicon, 1N4148	H-4	C-3	D-3	RF-28
CR504	Diode, Silicon, 1N4148	H-5	C-3	B-3	RF-28
CR505	Diode, Silicon, 1N4148	E-5	D-5	E-5	RF-28
F501	Fuse, Slo-Blo, 1/8A, 250V, 3AG	B-2	B-3	C-3	FU-20
J501	1793 Connector, IEEE	H-3	A-3	—	CS-377
J501	6423 Connector, IEEE	H-3	—	B-3	CS-324
J1003B	Connector Hsg, Female, 3 pin (Contacts CS-276)	B-1	B-2	C-5	CS-287-3
K501	Relay, 5V, Reed Type	B-4	C-3	D-3	RL-56
P1003A	Connector, Male, 3 Pin	A-1	B-3	C-3	CS-379-3
P1008	1793 Cable Assembly	A-4	D-1	—	CA-9-1
P1008	6423 Cable Assembly	A-4	—	E-1	CA-9-2
R501	Resistor, 47Ω, 5%, 1/4W, Composition	C-5	D-3	E-2	R-76-47
R502	Resistor, 10kΩ, 5%, 1/4W, Composition	C-6	E-3	F-2	R-76-10k
R503	Resistor, 100kΩ, 5%, 1/4W, Composition	C-6	E-3	F-3	R-76-100k
R504	Resistor, 2.4kΩ, 5%, 1/4W, Composition	H-4	C-3	D-3	R-76-2.4k
R505	Resistor, 2.4kΩ, 5%, 1/4W, Composition	H-5	C-3	D-3	R-76-2.4k
R506	Resistor, 6.2kΩ, 5%, 1/4W, Composition	H-4	C-3	D-3	R-76-6.2k
R507	Resistor, 6.2kΩ, 5%, 1/4W, Composition	H-6	C-3	D-3	R-76-6.2k
R508	Resistor, 100kΩ, 5%, 1/4W, Composition	C-6	D-3	E-3	R-76-100k
R509	Resistor, 150Ω, 5%, 1/4W, Composition	D-6	D-3	E-3	R-76-150
R510	Resistor, 10kΩ, 5%, 1/4W, Composition	C-6	D-3	E-3	R-76-10k
R511	Resistor, 10kΩ, 5%, 1/4W, Composition	D-6	D-3	E-3	R-76-10k
R512	Resistor, 10kΩ, 5%, Thick Film, Composition	SEV	E-5	F-5	TF-99
R513	Resistor, 56kΩ, 5%, 1/4W, Composition	E-5	D-5	E-5	R-76-56k
R514	Resistor, 100Ω, 10%, 1/2W, Composition (PC-581 only)				R-1-100
S501	Switch, Slide, Line Voltage Select	B-3	C-2	D-2	SW-397
S502	Switch, Dip	C-2	E-4	F-4	SW-377
T501	Transformer, Power	B-2	C-2	E-2	TR-178
U501	IC, CMOS, 8-Stage, Static Shift Register, CD4021AE	B-5	E-2	F-2	IC-130
U502	IC, CMOS, Hex Inverter, CD4049AE	SEV	D-2	E-2	IC-106
U503	IC, CMOS, Presettable, divide by N Counter, CD4018AE	A-4	E-2	F-2	IC-145
U504	IC, Bus Transceiver, MC3447P, (PC-524)	G-3	B-4	C-4	IC-229
U504	IC, Bus Transceiver SN75160A, (PC-581)	G-4	B-4	C-4	IC-298
U505	IC, Bus Transceiver, Quad Interface, MC3446AP	G-4	C-4	D-4	IC-134
U506	IC, Flip Flop, Dual "D", 74LS74	F-6, G-5	D-4	E-4	IC-144

Table 6-1. Model 1793/6423, Parts List (Cont.)

Circuit Desig.	Description	Schematic Location	PC-Board Location 1793	PC-Board Location 6423	Keithley Part No.
U507	IC, Hex, Inverting Schmitt Trigger, 7414	SEV	D-4	E-4	IC-153
U508	IC, Quad 2-Input NAND gate, 74LS00	SEV	D-4	E-4	IC-163
U509	IC, Peripheral Interface Adapter, 6821	E-4	C-4	D-4	LSI-8
U510	IC, Quad, 2-Input AND gate, 74LS08	SEV	D-4	E-4	IC-215
U511	IC, 8 Bit Microprocessor, 6802	D-4	C-5	D-5	LSI-18
U512	IC, Programmed, IC-220 for 1793/6423	E-1	D-5	E-5	PRO-103-01
U513	IC, Hex 3-State Buffer 74LS367	D-1	E-5	F-5	IC-161
VR501	+5V Voltage Regulator, 3 terminal, 7805	C-3	E-4	F-4	IC-93
Y501	Crystal, 4.0MHz	D-4	C-5	D-5	CR-10